

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT WE, YASUHIRO NIHEI, a citizen of Japan residing at Kanagawa, Japan, MASAAKI ISHIDA, a citizen of Japan residing at Kanagawa, Japan, ATSUFUMI OMORI, a citizen of Japan residing at Kanagawa, Japan, and DAN OZASA, a citizen of Japan residing at Kanagawa, Japan have invented certain new and useful improvements in

CIRCUIT FOR GENERATING PIXEL CLOCK
WITH FINE PHASE CONTROL

of which the following is a specification:

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to the generation and phase control of a pixel clock for use in laser printers, digital copiers, and other image forming apparatuses in general, and particularly relates to a pixel-clock generating circuit and an image forming apparatus having such a circuit wherein the pixel-clock generation circuit achieves highly precise phase control of a pixel clock.

2. Description of the Related Art

Fig. 25 is an illustrative drawing showing a general construction of an image forming apparatus such as a laser printer or a digital copier. In Fig. 25, a laser beam emitted by a semiconductor laser unit 1001 is scanned by a rotating polygon mirror 1002, and forms a light spot through a scan lens 1003 on a photoconductor 1004 serving as a medium to be scanned, thereby forming a latent image through the exposure of the photoconductor 1004 to light. For this purpose, a clock generating circuit 1008 generates a clock signal. Based on this clock signal, a phase synchronizing circuit 1009 generates an image clock signal (pixel clock) having

synchronized phase with respect to each line in response to an output signal of a photo-detector 1005. The image clock signal is supplied to an image-processing unit 1006 and a laser drive circuit 5 1007. With this provision, the laser drive circuit 1007 controls the timing of laser emission according to image data generated by the image-processing unit 1006 and the image clock signal having its phase controlled by the phase synchronizing circuit 1009 10 for each line, thereby controlling the latent image on the photoconductor 1004.

In this optical scan system, the deflection surfaces of a deflector such as a polygon scanner may have varying distances from the center 15 of rotation. Such variation causes fluctuation of scanning speed as the light spot (scan beam) scans over a target surface. The fluctuation of scanning speed results in fluctuation of images, causing degradation of image quality. When high image 20 quality is required, thus, the fluctuation of scanning needs to be corrected. In the case of a multi-beam optical system, a difference in the wavelengths of light sources results in the error of exposed positions where the optical system is not 25 corrected for chromatic aberration of the scan lens.

The width of scanning when the light spots of respective light sources scan over the target medium differs for each light source, causing degradation of image quality. This gives rise to a need for the 5 correction of scan widths.

As a conventional technology for correcting the fluctuation of scanning or the like, the position of a light spot is controlled along a scan line by changing the frequency of a pixel clock 10 as disclosed in Patent Document 1 and Patent Document 2.

[Patent Document 1] Japanese Patent Application Publication No. 11-167081

[Patent Document 2] Japanese Patent Application 15 Publication No. 2001-228415

However, the conventional scheme that changes the frequency of a pixel clock has a drawback in that the construction of a pixel-clock control unit becomes excessively complex, and that 20 such complexity increases as the step of frequency modulation becomes finer. This prohibits diligent frequency control.

Accordingly, there is a need for a pixel-clock generating circuit and an image forming 25 apparatus having such a circuit wherein pixel-clock

generating circuit has a simple construction for achieving the phase control of a pixel clock.

SUMMARY OF THE INVENTION

5 It is a general object of the present invention to provide a pixel-clock generating circuit and an image forming apparatus having such a circuit that substantially obviate one or more problems caused by the limitations and disadvantages
10 of the related art.

Features and advantages of the present invention will be presented in the description which follows, and in part will become apparent from the description and the accompanying drawings, or may be
15 learned by practice of the invention according to the teachings provided in the description. Objects as well as other features and advantages of the present invention will be realized and attained by a pixel-clock generating circuit and an image forming apparatus having such a circuit particularly pointed out in the specification in such full, clear, concise, and exact terms as to enable a person having ordinary skill in the art to practice the invention.

25 To achieve these and other advantages in

accordance with the purpose of the invention, the invention provides a circuit for generating a pixel clock for use in scanning a laser beam, including a high-frequency-clock generating circuit which 5 generates a high-frequency clock having a higher frequency than the pixel clock, and a control circuit which generates the pixel clock while shifting a phase of the pixel clock by a shift step proportional to a clock cycle of the high-frequency 10 clock in response to phase data indicative of timing and amounts of phase shifts.

An image forming apparatus includes a pixel-clock generating unit which generates a pixel clock, a laser drive unit which emits a laser beam 15 in response to the pixel clock and image data, a photoconductor, and a deflector which scans the laser beam on the photoconductor to form an image on the photoconductor, wherein the pixel-clock generating unit includes a high-frequency-clock generating circuit which generates a high-frequency 20 clock having a higher frequency than the pixel clock, and a control circuit which generates the pixel clock while shifting a phase of the pixel clock by a shift step proportional to a clock cycle of the 25 high-frequency clock in response to phase data

indicative of timing and amounts of phase shifts.

In the pixel-clock generating circuit and the image forming apparatus described above, the phase of the pixel clock is controlled by utilizing 5 the high-frequency clock so as to achieve a phase shift by increments of a shift step proportional to the clock cycle of the high-frequency clock. Also, the phase shift is controlled by the phase data. This provides for a simple circuit construction to 10 achieve the fine and diligent phase control of the pixel clock.

Other objects and further features of the present invention will be apparent from the following detailed description when read in 15 conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an illustrative drawing showing the overall construction of an embodiment of an 20 image forming apparatus that includes a pixel-clock generating circuit according to the invention;

Fig. 2 is a block diagram showing the construction of the pixel-clock generating circuit according to a first embodiment;

25 Fig. 3 is a circuit diagram showing an

example of the construction of a phase-synchronizing-signal generating circuit of Fig. 2;

Fig. 4 is a circuit diagrams showing another example of the construction of the phase-synchronizing-signal generating circuit;

Fig. 5 is a circuit diagram showing an example of the construction of a control-signal generating circuit of Fig. 2;

Fig. 6 is a circuit diagram showing an example of the construction of a pixel-clock controlling circuit of Fig. 2;

Fig. 7 is a circuit diagram showing another example of the construction of the pixel-clock controlling circuit of Fig. 2;

Fig. 8A is a diagram showing the relationship between phase shifts and phase data;

Fig. 8B is a diagram showing the relationship between the phase data and a signal to be selected;

Fig. 9 is a timing chart for explaining an operation from the inputting of a horizontal synchronizing signal to the outputting of a pixel clock;

Fig. 10 is a block diagram showing the overall construction of the pixel-clock generating

circuit according to a second embodiment;

Fig. 11 is a circuit diagram showing an example of the construction of a phase-synchronizing-signal generating circuit of Fig. 10;

5 Fig. 12 is a timing chart showing a case where a horizontal synchronizing signal falls during a "H" period of a high-frequency clock;

Fig. 13 is a timing chart showing a case where the horizontal synchronizing signal falls 10 during a "L" period of the high-frequency clock;

Fig. 14 is a circuit diagram showing another example of the construction of the phase-synchronizing-signal generating circuit of Fig. 9;

15 Fig. 15 is a timing chart showing a case where the horizontal synchronizing signal falls during a "H" period of the high-frequency clock;

Fig. 16 is a timing chart showing a case where the horizontal synchronizing signal falls during a "L" period of the high-frequency clock;

20 Fig. 17 is a timing chart showing a case where the horizontal synchronizing signal falls during a "H" period of the high-frequency clock;

Fig. 18 is a timing chart showing a case 25 where the horizontal synchronizing signal falls during a "L" period of the high-frequency clock;

Fig. 19 is a block diagram showing the overall construction of the pixel-clock generating circuit according to a third embodiment;

5 Fig. 20 is a diagram showing the relationship between phase shifts and phase data;

Fig. 21 is a circuit diagram showing an example of the construction of two control-signal generating circuits of Fig. 19;

10 Fig. 22 is a diagram showing a truth table of multiplexers;

Fig. 23 is a diagram showing a truth table of the control-data generating circuit;

15 Fig. 24 is a timing chart showing a case where the phase of a pixel clock is controlled according to the third embodiment;

Fig. 25 is an illustrative drawing showing a general construction of an image forming apparatus such as a laser printer or a digital copier; and

20 Fig. 26 is a diagram showing the correction of phase data based on a measured time difference.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

25 In the following, embodiments of the present invention will be described with reference

to the accompanying drawings.

Fig. 1 is an illustrative drawing showing the overall construction of an embodiment of an image forming apparatus that includes a pixel-clock generating circuit according to the invention. The image forming apparatus of Fig. 1 includes a semiconductor laser 201, which emits laser light for a desired duration under the control of a laser drive unit 150. The laser beam emitted from the semiconductor laser 201 is shaped by a collimator lens 202 and a cylinder lens 203. The shaped laser beam is then directed to a polygon mirror 204, and is reflected so as to scan over a photoconductor 208 in a periodic fashion. Before illuminating the photo conductor 208, the laser beam reflected by the polygon mirror 204 travels through an $f\theta$ lens 205, a mirror 207, and a toroidal lens 206 for proper positioning of an optical axis. The laser beam directed in this manner is shone on and forms a light spot on the photoconductor 20 serving as a scanned medium. As a result, an image (latent image) responsive to the output of the semiconductor laser 201 is formed on the photoconductor 208.

Photo-detectors 101 and 102 are provided at opposite ends of the mirror 207, respectively, so

as to detect the start and end of each scan. Namely, the laser beam reflected in a desired direction by the polygon mirror 204 is input into the photo-detector 101 before scanning one line over the 5 photoconductor 208, and is input into the photo-detector 102 after scanning one line. The photo-detectors 101 and 102 convert the incident laser light into electrical signals (i.e., first and second horizontal synchronizing signals), which are 10 supplied to a dot-position-error detecting and controlling unit 110. Thus, the dot-position-error detecting and controlling unit 110 receives a timing signal (the first horizontal synchronizing signal) indicative of the start of each scan line and a 15 timing signal (the second horizontal synchronizing signal) indicative of the end of each scan line. The first horizontal synchronizing signal output from the photo-detector 101 is also supplied to a pixel-clock generating unit 120 as a line 20 synchronizing signal.

The dot-position-error detecting and controlling unit 110 measures a time difference between the two electrical signals (the first and second horizontal synchronizing signals) supplied 25 from the photo-detectors 101 and 102, respectively.

Based on the measured time difference, an error of a scan time is obtained for each line. To this end, the measured time difference may be compared with a preset reference time length, or a similar method 5 may be employed.

The dot-position-error detecting and controlling unit 110 generates phase data for correction of the obtained error. The phase data may be used for correcting the fluctuation of 10 scanning caused by the characteristics of an optical system comprised of a scan lens and the like, for correcting the error of dot positions caused by the fluctuation of rotation of the polygon mirror 204, and/or for correcting the error of dot positions 15 caused by chromatic aberration of laser light. Such phase data contains instruction for a specific phase shift of the pixel clock. The generated phase data is supplied to the pixel-clock generating unit 120.

The pixel-clock generating unit 120 20 generates a pixel clock signal (PCLK) in phase synchronization with the first horizontal synchronizing signal output from the photo-detector 101. The pixel clock signal is used as a timing signal for driving the semiconductor laser 201 based 25 on the phase data supplied from the dot-position-

error detecting and controlling unit 110. The generated pixel clock (PCLK) is supplied to an image-processing unit 130 and a laser-drive-data generating unit 140. The pixel-clock generating unit 120 is a pixel-clock generating circuit of the invention, the detail of which will be described with reference to Fig. 2 and drawings subsequent thereto.

The image-processing unit 130 generates image data on the basis of the pixel clock (PCLK) supplied from the pixel-clock generating unit (pixel-clock generating circuit) 120, and supplies the image data to the laser-drive-data generating unit 140. The laser-drive-data generating unit 140 generates laser-drive data (modulation data) from the supplied image data on the basis of the pixel clock (PCLK) supplied from the pixel-clock generating unit (pixel-clock generating circuit) 120. The laser-drive data is provided to the laser drive unit 150. The laser drive unit 150 drives the semiconductor laser 201 according to the supplied laser-drive data (modulation data). This makes it possible to form an image on the photoconductor 208 free from the effect of fluctuation of scanning.

25 In the following, a description will be

given of various embodiments of the pixel-clock generating unit 120, i.e., the pixel-clock generating circuit of the invention, of the above-mentioned image forming apparatus with reference to 5 the drawings.

<Embodiment 1>

Fig. 2 is a block diagram showing the construction of the pixel-clock generating circuit according to a first embodiment. In Fig. 2, a 10 pixel-clock generating circuit 10 includes a high-frequency-clock generating circuit 11, a transition detecting circuit 12, a control-signal generating circuit 13, a pixel-clock controlling circuit 14, and a phase-synchronizing-signal generating circuit 15. 15.

The high-frequency-clock generating circuit 11 generates a high-frequency clock VCLK, which serves as a basis for the pixel clock PCLK. The phase-synchronizing-signal generating circuit 15 20 synchronizes the horizontal synchronizing signal supplied from an exterior with the high-frequency clock so as to output it as a phase synchronizing signal. The transition detecting circuit 12 detects a transition of the phase synchronizing signal or 25 the pixel clock. Specifically, the transition

detecting circuit 12 detects a positive or negative transition of the pixel clock PCLK, and, in response thereto, outputs a pulse signal having a width equal to one clock cycle of the high-frequency clock VCLK.

5 Moreover, the transition detecting circuit 12 detects a negative transition of the phase synchronizing signal, and, in response thereto, outputs a pulse signal having a width equal to one clock cycle of the high-frequency clock VCLK. The
10 control-signal generating circuit 13 outputs a control signal a and a control signal b based on the externally supplied phase data indicative of a phase shift of the pixel clock and the detection signal output from the transition detecting circuit 12.
15 The pixel-clock controlling circuit 14 controls the transition timing of the pixel clock PCLK based on the high-frequency clock VCLK, the control signal a, and the control signal b, thereby generating PLCK.

As previously described, the phase data
20 indicates a phase shift (i.e., the amount of phase shift) of the pixel clock for the purpose of correcting the fluctuation of scanning caused by the characteristics of a scan lens, for correcting the error of dot positions caused by the fluctuation of
25 rotation of a polygon mirror, and/or for correcting

the error of dot positions caused by chromatic aberration of laser light. In this embodiment, the phase data is comprised of 3 bits, which are related to the amount of phase shift as shown in Fig. 8A.

5 Fig. 3 is a circuit diagram showing an example of the construction of the phase-synchronizing-signal generating circuit 15 of Fig. 2. The phase-synchronizing-signal generating circuit 15 includes a shift register SR. The shift register SR 10 performs a shift operation in response to the high-frequency clock VCLK, and synchronizes the supplied horizontal synchronizing signal with the high-frequency clock VCLK for outputting as the phase synchronizing signal. In Fig. 3, the supplied 15 horizontal synchronizing signal is shifted so as to successively become S0, S1, and S2, with S2 being output as the phase synchronizing signal. The number of stages of the shift register SR controls a time interval between the inputting of the 20 horizontal synchronizing signal and the outputting of the pixel clock PCLK.

Fig. 4 is a circuit diagrams showing another example of the construction of the phase-synchronizing-signal generating circuit 15. The 25 phase-synchronizing-signal generating circuit 15 of

Fig. 4 includes a multi-stage shift register SR and a multiplexer MUX. The shift register SR performs a shift operation in response to the high-frequency clock VCLK. Outputs of respective stages of the 5 shift register SR are input into the multiplexer MUX for selection according to externally provided select data. With this provision, a time interval between the inputting of the horizontal synchronizing signal and the outputting of the pixel 10 clock PCLK is adjustable, rather than being fixed.

Fig. 5 is a circuit diagram showing an example of the construction of the control-signal generating circuit 13 of Fig. 2. The control-signal generating circuit 15 includes a shift register SR 15 and a multiplexer MUX. The shift register SR performs a shift operation in response to the high-frequency clock VCLK, thereby successively shifting the supplied detection signal as S0 through S9. An output S2 of an intermediate register stage is 20 extracted as the control signal a. Outputs S3-S9 of the subsequent register stages are input into the multiplexer MUX, so that one of these outputs is selected according to the phase data. The phase data and the output OUT selected by the multiplexer 25 MUX is related as shown in Fig. 8B. The output of

the multiplexer MUX is transmitted as the control signal b.

Fig. 6 is a circuit diagram showing an example of the construction of the pixel-clock controlling circuit 14 of Fig. 2. Fig. 7 is a circuit diagram showing another example of the construction of the pixel-clock controlling circuit 14 of Fig. 2. In Fig. 6, the pixel-clock controlling circuit 14 includes a JK-flip-flop (JK-FF), which outputs a "H" signal at a positive transition of the high-frequency clock VCLK when the control signal a is "H" and the control signal b is "L". When the control signal a is "L" and the control signal b is "H", the JK-flip-flop outputs a "L" signal at a positive transition of the high-frequency clock VCLK. The output of the JK flip-flop serves as the pixel clock PCLK. In Fig. 7, the pixel-clock controlling circuit 14 includes a D-flip-flop (D-FF), which outputs a "H" signal at a positive transition of the high-frequency clock VCLK when the control signal a is "H" and the control signal b is "L". When the control signal a is "L" and the control signal b is "H", the D-flip-flop outputs a "L" signal at a positive transition of the high-frequency clock VCLK. The output of the D-

flip-flop serves as the pixel clock PCLK.

In the following, a description will be given of the operation of the pixel-clock generating circuit of this embodiment with reference to a 5 timing chart of Fig. 9.

Fig. 9 shows an operation from the inputting of the horizontal synchronizing signal to the outputting of the pixel clock PCLK, the way the pixel clock PCLK is generated so as to have a duty 10 ratio of 50% equivalent to 8 clock cycles of the high-frequency clock VCLK (zero phase shift), the way the pixel clock PCLK is generated so as to have a phase advancement equivalent to a 1/8 of the 8 clock cycles of the high-frequency clock VCLK (+1 15 phase shift), and the way the pixel clock PCLK is generated so as to have a phase delay equivalent to a 1/8 of the 8 clock cycles of the high-frequency clock VCLK (-1 phase shift). The phase shift and the phase data are related as shown in Fig. 8A.

20 In what follows, an operation from the inputting of the horizontal synchronizing signal to the outputting of the pixel clock PCLK will be described first. In this example, the phase data is initially set to "3". In Fig. 9, the horizontal 25 synchronizing signal is input into the phase-

synchronizing-signal generating circuit 15 at timing A. In response, the phase synchronizing signal is output at timing B in synchronization with the high-frequency clock VCLK. The transition detecting 5 circuit 12 detects a negative transition of the phase synchronizing signal at timing B, thereby generating a detection signal. The detection signal is successively shifted by the shift register SR (Fig. 5) of the control-signal generating circuit 13. 10 The outputs of respective stages of the shift register SR are shown as S0-S9 in Fig. 9. Since the control signal a is S2, the control signal a becomes "H" at timing C. Since the control signal a is "H" at clock timing D, the pixel-clock controlling 15 circuit 14 shown in Fig. 6 or Fig. 7 changes the pixel clock PCLK from "H" to "L". Since the phase data is "3", the control-signal generating circuit 13 outputs S6 as the control signal b from the multiplexer MUX of Fig. 5, as required by the 20 relationship of Fig. 8B. The control signal b thus becomes "H" at timing E. Since the control signal b is "H" at clock timing F, the pixel-clock controlling circuit 14 shown in Fig. 6 or Fig. 7 changes the pixel clock PCLK from "L" to "H". 25 In this manner, a time interval from the

inputting of the horizontal synchronizing signal to the outputting of the pixel clock PCLK is controlled with a margin of error smaller than one clock cycle of the high-frequency clock.

5 In what follows, a subsequent operation that generates the pixel clock PCLK will be described. A description will be given first of an operation that generates PCLK with a zero phase shift. When PCLK with a zero phase shift is to be
10 generated, phase data "3" is provided in synchronization with a positive transition of PCLK, (timing F shown in Fig. 9). The transition detecting circuit 12 detects the positive transition of PCLK at timing F, thereby generating a detection
15 signal. The control-signal generating circuit 13 successively shifts the detection signal by use of the shift register SR of Fig. 5. The outputs of respective stages of the shift register SR are shown as S0-S9 in Fig. 9. Since the control signal a is
20 S2, the control signal a becomes "H" at timing G. Since the control signal a is "H" at clock timing H, the pixel-clock controlling circuit 14 shown in Fig. 6 or Fig. 7 changes the pixel clock PCLK from "H" to "L". Since the phase data is "3", the control-
25 signal generating circuit 13 outputs S6 as the

control signal b from the multiplexer MUX of Fig. 5, as required by the relationship of Fig. 8B. The control signal b thus becomes "H" at timing I. Since the control signal b is "H" at clock timing J, 5 the pixel-clock controlling circuit 14 shown in Fig. 6 or Fig. 7 changes the pixel clock PCLK from "L" to "H". In this manner, the pixel clock PCLK having a zero phase shift is generated.

In the following, a description will be 10 given of an operation that generates PCLK with a phase shift "-1". When PCLK with a phase shift "-1" is to be generated, phase data "2" is provided in synchronization with a positive transition of PCLK, (timing J shown in Fig. 9). The transition 15 detecting circuit 12 detects the positive transition of PCLK at timing J, thereby generating a detection signal. The control-signal generating circuit 13 successively shifts the detection signal by use of the shift register SR of Fig. 5, thereby generating 20 S0-S9. Since the control signal a is S2, the control signal a becomes "H" at timing K. Since the control signal a is "H" at clock timing L, the pixel-clock controlling circuit 14 shown in Fig. 6 or Fig. 7 changes the pixel clock PCLK from "H" to 25 "L". Since the phase data is "2", the control-

signal generating circuit 13 outputs S5 as the control signal b from the multiplexer MUX of Fig. 5, as required by the relationship of Fig. 8B. The control signal b thus becomes "H" at timing M.

5 Since the control signal b is "H" at clock timing N, the pixel-clock controlling circuit 14 shown in Fig. 6 or Fig. 7 changes the pixel clock PCLK from "L" to "H". In this manner, the pixel clock PCLK having a phase shift "-1" is generated.

10 In the following, a description will be given of an operation that generates PCLK with a phase shift "+1". When PCLK with a phase shift "+1" is to be generated, phase data "4" is provided in synchronization with a positive transition of PCLK,

15 (timing N shown in Fig. 9). The transition detecting circuit 12 detects the positive transition of PCLK at timing N, thereby generating a detection signal. The control-signal generating circuit 13 successively shifts the detection signal by use of

20 the shift register SR of Fig. 5, thereby generating S0-S9. Since the control signal a is S2, the control signal a becomes "H" at timing O. Since the control signal a is "H" at clock timing P, the pixel-clock controlling circuit 14 shown in Fig. 6

25 or Fig. 7 changes the pixel clock PCLK from "H" to

"L". Since the phase data is "4", the control-signal generating circuit 13 outputs S7 as the control signal b from the multiplexer MUX of Fig. 5, as required by the relationship of Fig. 8B. The 5 control signal b thus becomes "H" at timing Q. Since the control signal b is "H" at clock timing R, the pixel-clock controlling circuit 14 shown in Fig. 6 or Fig. 7 changes the pixel clock PCLK from "L" to "H". In this manner, the pixel clock PCLK having a 10 phase shift "+1" is generated.

In the manner as described above, phase data is provided in synchronization with the pixel clock PCLK so as to change the phase of the pixel clock PCLK with respect to each clock cycle.

15 <Embodiment 2>

Fig. 10 is a block diagram showing the overall construction of the pixel-clock generating circuit according to a second embodiment. In Fig. 10, the pixel-clock generating circuit 10 includes 20 the high-frequency-clock generating circuit 11, the transition detecting circuit 12, the control-signal generating circuit 13, the clock generating circuit 14, a transition detecting circuit 115, a control-signal generating circuit 16, a clock generating 25 circuit 17, a multiplexer (MUX) 18, and a phase-

synchronizing-signal generating circuit 19.

The high-frequency-clock generating circuit 11 generates a high-frequency clock VCLK, which serves as a basis for the pixel clock PCLK.

5 The transition detecting circuit 12 operates in response to a positive transition of the high-frequency clock VCLK to detect a positive transition of a first clock signal and a negative transition of a first phase synchronizing signal, thereby

10 outputting a pulse signal having a width equal to one clock cycle of the high-frequency clock VCLK. The output of the transition detecting circuit 12 is a first detection signal. The control-signal generating circuit 13 operates in response to a

15 positive transition of the high-frequency clock VCLK to generate a control signal 1a and a control signal 1b based on the output of the transition detecting circuit 12 and the phase data. The clock generating circuit 14 operates in response to a positive

20 transition of the high-frequency clock VCLK to generate a first clock based on the control signal 1a and the control signal 1b. The transition detecting circuit 115 operates in response to a negative transition of the high-frequency clock VCLK

25 to detect a positive transition of a second clock

signal and a negative transition of a second phase synchronizing signal, thereby generating a pulse signal having a width equal to one clock cycle of of the high-frequency clock VCLK. The output of the 5 transition detecting circuit 115 is a second detection signal. The control-signal generating circuit 16 operates in response to a negative transition of the high-frequency clock VCLK to output a control signal 2a and a control signal 2b 10 based on the output of the transition detecting circuit 115 and the phase data. The clock generating circuit 17 operates in response to a negative transition of the high-frequency clock VCLK to generate a second clock based on the control 15 signal 2a and the control signal 2b. The multiplexer 18 selects one of the first clock and the second clock in accordance with a phase state signal supplied from the phase-synchronizing-signal generating circuit 19, and outputs the selected 20 clock signal as the pixel clock PCLK.

The phase-synchronizing-signal generating circuit 19 receives a horizontal synchronizing signal, and outputs the first phase synchronizing signal synchronized with a positive transition of 25 the high-frequency clock VCLK, the second phase

synchronizing signal synchronized with a negative transition of the high-frequency clock VCLK, and the phase state signal indicative of timing of the horizontal synchronizing signal, i.e., indicative of 5 whether horizontal synchronizing signal falls during the "H" period of the high-frequency clock VCLK or falls during the "L" period of the high-frequency clock VCLK.

As previously described, the phase data 10 indicates a phase shift (i.e., the amount of phase shift) of the pixel clock for the purpose of correcting the fluctuation of scanning caused by the characteristics of a scan lens, for correcting the error of dot positions caused by the fluctuation of 15 rotation of a polygon mirror, and/or for correcting the error of dot positions caused by chromatic aberration of laser light. In this embodiment, the phase data is comprised of 3 bits, which are related to the amount of phase shift as shown in Fig. 8A.

20 Fig. 11 is a circuit diagram showing an example of the construction of the phase-synchronizing-signal generating circuit 19 of Fig. 10. The phase-synchronizing-signal generating circuit 19 includes shift registers. A shift 25 register SR1 comprised of flip-flops FF10 through

FF12 performs a shift operation in response to a positive transition of the high-frequency clock VCLK, and synchronizes the supplied horizontal synchronizing signal with a positive transition of 5 the high-frequency clock VCLK for outputting an output Q12 of FF12 as the first phase synchronizing signal. A shift register SR2 comprised of flip-flops FF20 through FF22 performs a shift operation in response to a negative transition of the high- 10 frequency clock VCLK, and synchronizes the supplied horizontal synchronizing signal with a negative transition of the high-frequency clock VCLK for outputting an output Q22 of F22 as the second phase synchronizing signal.

15 Moreover, the phase-synchronizing-signal generating circuit 19 includes a sequential circuit 19A inclusive of a RS-FF for generating the phase state signal indicative of input timing of the horizontal synchronizing signal. An operation that 20 generate the phase state signal will be described with reference to Fig. 12 and Fig. 13.

Fig. 12 is a timing chart showing a case where the horizontal synchronizing signal falls during a "H" period (timing A) of the high-frequency 25 clock VCLK. In this case, signals A1 and A2 are

output at timing C and timing B, respectively, as shown in Fig. 12. In response, a SET signal (S in Fig. 11) becomes "H" at timing B, so that the output of RS-FF, i.e., the phase state signal, is set to 5 "H". Thereafter, a RESET signal (R in Fig. 11) is set to "H" at timing D, so that the output of RS-FF, i.e., the phase state signal, is set to "L". In this manner, where the horizontal synchronizing signal falls during a "H" period of the high-frequency 10 clock VCLK, the phase state signal is set to "L".

Fig. 13 is a timing chart showing a case where the horizontal synchronizing signal falls during a "L" period (timing A) of the high-frequency 15 clock VCLK. In this case, the signals A1 and A2 are output at timing B and timing C, respectively, as shown in Fig. 13. In response, the RESET signal (R in Fig. 11) becomes "H" at timing B, so that the output of RS-FF, i.e., the phase state signal, is 20 set to "L". Thereafter, the SET signal (S in Fig. 11) is set to "H" at timing D, so that the output of RS-FF, i.e., the phase state signal, is set to "H". In this manner, where the horizontal synchronizing signal falls during a "L" period of the high-frequency 25 clock VCLK, the phase state signal is set

to "H".

Fig. 14 is a circuit diagram showing another example of the construction of the phase-synchronizing-signal generating circuit 19 of Fig. 9.

5 In the phase-synchronizing-signal generating circuit 19 of Fig. 14, circuitry for generating the phase state signal includes a sequential circuit and a T-FF. In this construction, a flip-flop FF13 is additionally provided for the shift register 10 comprised of FF10-FF12 in Fig. 11, and the signal A1 is generated by performing an AND operation between Q13 and Q12B. An operation by the phase-synchronizing-signal generating circuit 19 for generating the phase state signal is illustrated in 15 Fig. 15 and Fig. 16.

Fig. 15 is a timing chart showing a case where the horizontal synchronizing signal falls during a "H" period (timing A) of the high-frequency clock VCLK. First, T-FF is reset in response to the 20 detection of inputting of the horizontal synchronizing signal, thereby setting the phase state signal to "L". Then, the signals A2 and A1 are output at timing B and timing C of Fig. 15, respectively. A signal T is generated by performing 25 an AND operation between the signal A1 and the

signal A2. Since (A1, A2) never become (H, H) in this case, the signal T remains "L", resulting the output of T-FF also staying "L". The phase state signal is thus "L".

5 Fig. 16 is a timing chart showing a case where the horizontal synchronizing signal falls during a "L" period (timing A) of the high-frequency clock VCLK. First, T-FF is reset in response to the detection of inputting of the horizontal 10 synchronizing signal, thereby setting the phase state signal to "L". Then, the signals A2 and A1 are output at timing B and timing C of Fig. 16, respectively. The signal T is generated by performing an AND operation between the signal A1 15 and the signal A2. Since (A1, A2) becomes (H, H) at timing C in this case, the signal T is changed to "L". As the signal T is set to "H", the output of T-FF is toggled to become "H". As a result, the phase state signal is set to "H".

20 In the phase-synchronizing-signal generating circuit 19 shown in Fig. 11 and Fig. 14, the outputs of respective stages of a shift register may be provided to a multiplexer for selection as in the case of the phase-synchronizing-signal 25 generating circuit 15 shown in Fig. 4. With this

provision, a time interval between the inputting of the horizontal synchronizing signal and the outputting of the pixel clock PCLK is adjustable, rather than being fixed.

5 The control-signal generating circuit 13 and the control-signal generating circuit 16 shown in Fig. 10 have a circuit construction the same as that of Fig. 5. It should be noted, however, that the control-signal generating circuit 13 operates in 10 response to a positive transition of the high-frequency clock VCLK, and the control-signal generating circuit 16 operates in response to a negative transition of the high-frequency clock VCLK.

15 The clock generating circuit 14 and the clock generating circuit 17 shown in Fig. 10 have a circuit construction the same as that of Fig. 6 or Fig. 7. It should be noted, however, that the clock generating circuit 14 operates in response to a positive transition of the high-frequency clock VCLK, 20 and the clock generating circuit 17 operates in response to a negative transition of the high-frequency clock VCLK.

25 The first clock signal in Fig. 10 is generated from the system of the transition detecting circuit 12, the control-signal generating

circuit 13, and the clock generating circuit 14. The way the first clock signal is generated is the same as in the first embodiment, and the first clock signal is in synchronization with positive 5 transitions of the high-frequency clock VCLK. The second clock signal in Fig. 10 is generated from the system of the transition detecting circuit 115, the control-signal generating circuit 16, and the clock generating circuit 17. The way the second clock 10 signal is generated is the same as in the first embodiment, but the second clock signal is in synchronization with negative transitions of the high-frequency clock VCLK.

The horizontal synchronizing signal, the 15 first clock, the second clock, and the pixel clock PCLK in the pixel-clock generating circuit 10 of Fig. 10 are illustrated in Fig. 17 and Fig. 18.

Fig. 17 is a timing chart showing a case where the horizontal synchronizing signal falls 20 during a "H" period of the high-frequency clock VCLK. Since the horizontal synchronizing signal falls during the "H" period of the high-frequency clock VCLK (timing A of Fig. 17), the phase state signal is set to "L". Consequently, the multiplexer 18 of 25 Fig. 10 selects the first clock for outputting as

the pixel clock PCLK (timing B of Fig. 17).

Fig. 18 is a timing chart showing a case where the horizontal synchronizing signal falls during a "L" period of the high-frequency clock VCLK.

5 Since the horizontal synchronizing signal falls during the "L" period of the high-frequency clock VCLK (timing A of Fig. 18), the phase state signal is set to "H". Consequently, the multiplexer 18 of Fig. 10 selects the second clock for outputting as 10 the pixel clock PCLK (timing B of Fig. 18).

In the second embodiment as described above, a time interval between the inputting of the horizontal synchronizing signal and the outputting of the pixel clock PCLK is controlled with a margin 15 of error smaller than half a clock cycle of the high-frequency clock. Moreover, the provision of phase data makes it possible to change the phase of the pixel clock PCLK by a step size equal to one clock cycle of the high-frequency clock VCLK.

20 <Embodiment 3>

Fig. 19 is a block diagram showing the overall construction of the pixel-clock generating circuit according to a third embodiment. In Fig. 19, the pixel-clock generating circuit 10 includes the 25 high-frequency-clock generating circuit 11, the

transition detecting circuit 12, the control-signal generating circuit 13, the clock generating circuit 14, the transition detecting circuit 115, the control-signal generating circuit 16, the clock generating circuit 17, the multiplexer (MUX) 18, a control-data generating circuit 119, a status-signal generating circuit 20, a select-signal generating circuit 21, and a phase-synchronizing-signal generating circuit 22.

10 The high-frequency-clock generating circuit 11 generates a high-frequency clock VCLK, which serves as a basis for the pixel clock PCLK. The transition detecting circuit 12 operates in response to a positive transition of the high-frequency clock VCLK to detect a positive transition of a first clock signal, thereby outputting a pulse signal having a width equal to one clock cycle of the high-frequency clock VCLK. The control-signal generating circuit 13 operates in response to a 15 positive transition of the high-frequency clock VCLK to generate the control signal 1a and the control signal 1b based on the output of the transition detecting circuit 12 and first control data supplied from the control -data generating circuit 119. The 20 clock generating circuit 14 operates in response to 25

a positive transition of the high-frequency clock VCLK to generate the first clock based on the control signal 1a and the control signal 1b. The transition detecting circuit 115 operates in response to a negative transition of the high-frequency clock VCLK to detect a positive transition of the second clock signal, thereby generating a pulse signal having a width equal to one clock cycle of the high-frequency clock VCLK. The control-
10 signal generating circuit 16 operates in response to a negative transition of the high-frequency clock VCLK to output the control signal 2a and the control signal 2b based on the output of the transition detecting circuit 115 and second control data supplied from the control-data generating circuit 119. The clock generating circuit 17 operates in response to a negative transition of the high-frequency clock VCLK to generate the second clock based on the control signal 2a and the control signal 2b. The multiplexer 18 selects one of the first clock and the second clock in accordance with a select signal supplied from the select-signal generating circuit 21, and outputs the selected clock signal as the pixel clock PCLK.

25 The control-data generating circuit 119

generates the first control data and the second control data based on the phase data supplied from an exterior and the status signal supplied from the status-signal generating circuit 20. As previously 5 described, the phase data indicates a phase shift (i.e., the amount of phase shift) of the pixel clock for the purpose of correcting the fluctuation of scanning caused by the characteristics of a scan lens, for correcting the error of dot positions 10 caused by the fluctuation of rotation of a polygon mirror, and/or for correcting the error of dot positions caused by chromatic aberration of laser light. In this embodiment, the phase data is comprised of 3 bits, which are related to the amount 15 of phase shift as shown in Fig. 20.

The status-signal generating circuit 20 toggles its output at timing of a positive transition of the pixel clock PCLK when bit0 of the phase data is 1, thereby generating the status 20 signal. As a result, the status signal indicates a first state when the pixel clock PCLK falls at a positive transition of the high-frequency clock VCLK, and indicates a second state when the pixel clock PCLK falls at a negative transition of the high- 25 frequency clock VCLK. In this embodiment, the

status signal is "0" when the pixel clock PCLK falls at a positive transition of the high-frequency clock VCLK, and is "1" when the pixel clock PCLK falls at a negative transition of the high-frequency clock 5 VCLK. An initial value of the status signal is determined based on the phase state signal supplied from the phase-synchronizing-signal generating circuit 22.

The select-signal generating circuit 21 10 toggles its output at timing of a negative transition of the pixel clock PCLK when bit0 of the phase data is 1, thereby generating the select signal. An initial value of the select signal is determined based on the phase state signal supplied 15 from the phase-synchronizing-signal generating circuit 22.

The clock generating circuit 14 and the clock generating circuit 17 in Fig. 19 have a construction the same as that of Fig. 6 or Fig. 7.

20 Fig. 21 is a circuit diagram showing an example of the construction of the control-signal generating circuit 13 and the control-signal generating circuit 16 of Fig. 19. The control-signal generating circuit 13 and the control-signal generating circuit 16 each includes a shift register 25

and a multiplexer. The shift register SR-1 of the control-signal generating circuit 13 performs a shift operation in response to a positive transition of the high-frequency clock VCLK, and the shift 5 register SR-2 of the control-signal generating circuit 16 performs a shift operation in response to a negative transition of the high-frequency clock VCLK. The shift register SR-1 successively shifts the supplied first detection signal as S10 through 10 S18, and extracts an output S12 of an intermediate register stage as the control signal 1a. The shift register SR-2 successively shifts the supplied first detection signal as S20 through S28, and extracts an output S22 of an intermediate register stage as the 15 control signal 2a. Outputs S14-S18 of the subsequent register stages of the shift register SR-1 are input into the multiplexer MUX-1, and outputs S24-S28 of the subsequent register stages of the shift register SR-2 are input into the multiplexer 20 MUX-2. The multiplexer MUX-1 selects one of the register outputs S14-S18 according to the first control data supplied from the control-data generating circuit 119, and outputs the selected signal as the control signal 1b. The multiplexer 25 MUX-2 selects one of the register outputs S24-S28

according to the second control data supplied from the control-data generating circuit 119, and outputs the selected signal as the control signal 2b. Fig. 22 is a diagram showing a truth table of the 5 multiplexer MUX-1 and the multiplexer MUX-2.

In the following, a description will be given of the control-data generating circuit 119 of Fig. 19. The control-data generating circuit 119 decodes the phase data supplied from an exterior and 10 the status signal supplied from the status-signal generating circuit 20, thereby outputting the first control data and the second control data. Operation of the control-data generating circuit 119 is related to the control-signal generating circuit 13 15 and the control-signal generating circuit 16. That is, the decoding operation performed by the control-data generating circuit 119 varies depending on an order in which the outputs of the shift registers SR-1 and SR-2 and the inputs of the multiplexer MUX- 20 1 and the multiplexer MUX-2 are provided in the control-signal generating circuit 13 and the control-signal generating circuit 16. In this embodiment, the amount of phase shift and the phase data are related as shown in Fig. 20. Fig. 23 is a 25 diagram showing a truth table of the control-data

generating circuit 119 of this case.

The phase-synchronizing-signal generating circuit 22 in Fig. 19 has a construction the same as that of the second embodiment (Fig. 11). According 5 to the phase state signal supplied from the phase-synchronizing-signal generating circuit 22, one of the first clock and the second clock is selected as the pixel clock PCLK that is output for the first time after the inputting of the horizontal 10 synchronizing signal. Further, a time interval between the inputting of the horizontal synchronizing signal and the outputting of the pixel clock PCLK is controlled with a margin of error smaller than half a clock cycle of the high- 15 frequency clock signal.

In the following, the generation of the pixel clock PCLK after the generation of a first clock pulse in the pixel-clock generating circuit 10 of the third embodiment will be described with 20 reference to Fig. 24. Fig. 24 is a timing chart showing a case where the pixel clock PCLK is generated to have a clock cycle equivalent to 8 clock cycles of the high-frequency clock VCLK in the case of a zero phase shift, and, then, the pixel 25 clock PCLK is generated so as to have +1/16 phase

shift and then to have -1/16 phase shift.

A description will be given first of the generation of the pixel clock PCLK having a zero phase shift.

5 <Generation of First Control Data and Second Control Data>

Phase data "000" indicative of a zero phase shift is provided in synchronization with the pixel clock PCLK (timing A of Fig. 24). The phase data and the status signal (indicating "0" at the 10 beginning) are supplied to the control-data generating circuit 119, which generates the first control data "010" and the second control data "010" according to the truth table of Fig. 23.

<Generation of First Clock>

15 At timing A of Fig. 24, the transition detecting circuit 12 detects a positive transition of the first clock, thereby generating the first detection signal having a pulse width equal to one clock cycle of the high-frequency clock VCLK. The 20 first detection signal is supplied to the shift register SR-1 of the control-signal generating circuit 13 (Fig. 21), resulting in the register outputs S10-S18 being obtained as shown in Fig. 24. The control signal 1a that is the register output 25 S12 is set to "H" at timing B. Since the control

signal 1a is "H" at clock timing C, the clock generating circuit 14 changes the first clock to "L". Since the first control data is "010", the register output S16 appears at the output of the multiplexer 5 MUX-1 of the control-signal generating circuit 13 as the control signal 1b, which becomes "H" at timing D. Since the control signal 1b is "H" at clock timing E, the clock generating circuit 14 changes the first clock to "H".

10 <Generation of Second Clock>

At timing A' of Fig. 24, the transition detecting circuit 115 detects a positive transition of the second clock, thereby generating the second detection signal having a pulse width equal to one clock cycle of the high-frequency clock VCLK. The second detection signal is supplied to the shift register SR-2 of the control-signal generating circuit 16 (Fig. 21), resulting in the register outputs S20-S28 being obtained as shown in Fig. 24.

The control signal 2a that is the register output S22 is set to "H" at timing B'. Since the control signal 2a is "H" at clock timing C', the clock generating circuit 17 changes the second clock to "L". Since the second control data is "010", the register output S26 appears at the output of the

multiplexer MUX-2 of the control-signal generating circuit 16 as the control signal 2b, which becomes "H" at timing D'. Since the control signal 2b is "H" at clock timing E', the clock generating circuit 5 17 changes the second clock to "H".

<Generation of Pixel Clock PCLK>

Since the select signal is "L", the first clock is output as the pixel clock PCLK.

A description will now be given of the 10 generation of the pixel clock PCLK having a +1/16 phase shift.

<Generation of First Control Data and Second Control Data>

Phase data "001" indicative of a "+1" phase shift is provided in synchronization with the 15 pixel clock PCLK (timing E of Fig. 24). As bit0 of the immediately preceding phase data is "0", the status signal output from the status-signal generating circuit 20 is not toggled, staying at "0". The phase data and the status signal are supplied to 20 the control-data generating circuit 119, which generates the first control data "010" and the second control data "001" according to the truth table of Fig. 23.

<Generation of First Clock>

25 At timing E of Fig. 24, the transition

detecting circuit 12 detects a positive transition of the first clock, thereby generating the first detection signal having a pulse width equal to one clock cycle of the high-frequency clock VCLK. The 5 first detection signal is supplied to the shift register SR-1 of the control-signal generating circuit 13 (Fig. 21), resulting in the register outputs S10-S18 being obtained as shown in Fig. 24. The control signal 1a that is the register output 10 S12 is set to "H" at timing F. Since the control signal 1a is "H" at clock timing G, the clock generating circuit 14 changes the first clock to "L". Since the first control data is "010", the register output S16 appears at the output of the multiplexer 15 MUX-1 of the control-signal generating circuit 13 as the control signal 1b, which becomes "H" at timing H. Since the control signal 1b is "H" at clock timing I, the clock generating circuit 14 changes the first clock to "H".

20 **<Generation of Second Clock>**

At timing E' of Fig. 24, the transition detecting circuit 115 detects a positive transition of the second clock, thereby generating the second detection signal having a pulse width equal to one 25 clock cycle of the high-frequency clock VCLK. The

second detection signal is supplied to the shift register SR-2 of the control-signal generating circuit 16 (Fig. 21), resulting in the register outputs S20-S28 being obtained as shown in Fig. 24.

5 The control signal 2a that is the register output S22 is set to "H" at timing F'. Since the control signal 2a is "H" at clock timing G', the clock generating circuit 17 changes the second clock to "L". Since the second control data is "001", the 10 register output S27 appears at the output of the multiplexer MUX-2 of the control-signal generating circuit 16 as the control signal 2b, which becomes "H" at timing H'. Since the control signal 2b is "H" at clock timing I', the clock generating circuit 17 changes the second clock to "H".

<Generation of Pixel Clock PCLK>

Since bit0 of the phase data is "1", the select signal is toggled at timing G corresponding to a negative transition of the pixel clock PCLK, 20 thereby changing to "1". As a result, the multiplexer 18 initially outputs the first clock as the pixel clock PCLK (during the period from timing E to timing G of Fig. 24), and then outputs the second clock as the pixel clock PCLK (during the 25 period from timing G to timing I' of Fig. 24) after

the change to "1" of the select signal.

A description will now be given of the generation of the pixel clock PCLK having a -1/16 phase shift.

5 <Generation of First Control Data and Second Control Data>

Phase data "111" indicative of a "-1" phase shift is provided in synchronization with the pixel clock PCLK (timing I' of Fig. 24). As bit0 of the immediately preceding phase data is "1", the 10 status signal output from the status-signal generating circuit 20 is toggled, changing to "1" (timing I' of Fig. 24). The phase data and the status signal are supplied to the control-data generating circuit 119, which generates the first 15 control data "010" and the second control data "011" according to the truth table of Fig. 23.

<Generation of First Clock>

At timing I of Fig. 24, the transition detecting circuit 12 detects a positive transition 20 of the first clock, thereby generating the first detection signal having a pulse width equal to one clock cycle of the high-frequency clock VCLK. The first detection signal is supplied to the shift register SR-1 of the control-signal generating 25 circuit 13 (Fig. 21), resulting in the register

outputs S10-S18 being obtained as shown in Fig. 24. The control signal 1a that is the register output S12 is set to "H" at timing J. Since the control signal 1a is "H" at clock timing K, the clock generating circuit 14 changes the first clock to "L". Since the first control data is "010", the register output S16 appears at the output of the multiplexer MUX-1 of the control-signal generating circuit 13 as the control signal 1b, which becomes "H" at timing L. Since the control signal 1b is "H" at clock timing M, the clock generating circuit 14 changes the first clock to "H".

<Generation of Second Clock>

At timing I' of Fig. 24, the transition detecting circuit 115 detects a positive transition of the second clock, thereby generating the second detection signal having a pulse width equal to one clock cycle of the high-frequency clock VCLK. The second detection signal is supplied to the shift register SR-2 of the control-signal generating circuit 16 (Fig. 21), resulting in the register outputs S20-S28 being obtained as shown in Fig. 24. The control signal 2a that is the register output S22 is set to "H" at timing J'. Since the control signal 2a is "H" at clock timing K', the clock

generating circuit 17 changes the second clock to "L". Since the second control data is "011", the register output S25 appears at the output of the multiplexer MUX-2 of the control-signal generating 5 circuit 16 as the control signal 2b, which becomes "H" at timing L'. Since the control signal 2b is "H" at clock timing M', the clock generating circuit 17 changes the second clock to "H".

<Generation of Pixel Clock PCLK>

10 Since bit0 of the phase data is "1", the select signal is toggled at timing K' corresponding to a negative transition of the pixel clock PCLK, thereby changing to "0". As a result, the multiplexer 18 initially outputs the second clock as 15 the pixel clock PCLK (during the period from timing I' to timing K' of Fig. 24), and then outputs the first clock as the pixel clock PCLK (during the period from timing K' to timing M of Fig. 24) after the change to "0" of the select signal.

20 The above description has been provided with reference to a case where a phase shift is 0, +1/16 (i.e., +1/16 of one clock cycle of PCLK), and -1/16 (i.e., -1/16 of one clock cycle of PCLK). It should be noted that other phase shifts such as 25 +2/16, +3/16, -2/16, and -3/16 can as well be made

in the same manner.

In the manner as described above, the pixel clock PCLK is given a phase shift with respect to each clock cycle where the phase shift is made by 5 a shift step equal to $\pm 1/16$ of the clock cycle, i.e., by a shift step equal to half the clock cycle of the high-frequency clock VCLK.

In the following, a description will be given with regard to the correction of phase data.

10 As previously described in connection with Fig. 1, the dot-position-error detecting and controlling unit 110 generates the phase data.

In the present invention, the dot-position-error detecting and controlling unit 110 15 measures a time difference between the two electrical signals (the first and second horizontal synchronizing signals) supplied from the photo-detectors 101 and 102, respectively, thereby obtaining an actual scan time. Based on the 20 actually measured scan time, feedback correction may be made to the phase data.

For the sake of explanation, a configuration in which one line is comprised of 4800 dots is taken as an example. Fig. 26 is a diagram 25 showing the correction of phase data based on a

measured time difference.

In Fig. 26, phase data 200 that is initially stored in memory is aimed at correcting the fluctuation of scanning speed that is faster near the start and near the end and is slower in the middle. If the measured scan time (i.e., a time difference between the first horizontal synchronizing signal and the second horizontal synchronizing signal) is longer than expected, phase-data correction data 201 may be added to the phase data 200, thereby generating new phase data (corrected phase data) 202. This correction is made by adding a "+1" phase shift once in every ten dots.

With such correction of phase data through feedback control, more accurate phase control may be achieved.

Further, the present invention is not limited to these embodiments, but various variations and modifications may be made without departing from the scope of the present invention.

The present application is based on Japanese priority application No. 2003-031057 filed on February 7, 2003, with the Japanese Patent Office, the entire contents of which are hereby incorporated by reference.